

* NOTICES *

JP - 2000 200688

Japan Patent Office is not responsible for any damages caused by the use of this translation.

1. This document has been translated by computer. So the translation may not reflect the original precisely.
2. **** shows the word which can not be translated.
3. In the drawings, any words are not translated.

DETAILED DESCRIPTION

[Detailed Description of the Invention]

[0001]

[The technical field to which invention belongs] Especially this invention is applied to the semiconductor device which formed a vertical-mold bipolar transistor, and SOI [perfect depletion type] and MISFET in the same substrate about a semiconductor device and its manufacturing technology, and relates to effective technology.

[0002]

[Description of the Prior Art] In addition to the demand of high integration with the semiconductor device applied in the remarkable high-speed communication field of development, the demand of improvement in the speed and low-power-izing is strong in recent years. Vertical-mold bipolar transistor structure is known as device structure where a high-speed performance may be filled, and C-MISFET (Complementary-Metal Insulator Semiconductor Field Effect Transistor) structure is known as device structure where a low-power performance may be filled. Moreover, MISFET reduces substrate capacity by forming in a SOI (Silicon On Insulator) substrate, and it is known that highly efficient-ization can be attained. Then, Bi-CMOS device which forms a bipolar transistor and C-MISFET on the same SOI substrate is considered. Such a Bi-CMOS device combines the rapidity of a bipolar transistor, and the low-power nature of C-MISFET, and since it has the feature that it is still stronger also to the soft error by alpha rays, it has a great hope as a semiconductor device which may fill the needs in the aforementioned high-speed communication field.

[0003] for example, T.kikuchi et al., A 0.35 um ECL-CMOS Process Technology on SOI for 1 second Mega-bits SRAMs with 40ps Gate Array, IEDM Technical Digest, pp.923-926, and 1995. **** -- Bi-CMOS device formed in the SOI substrate is indicated In this Bi-CMOS device, a high-speed vertical-mold bipolar transistor and high-speed MISFET are formed in a single SOI layer, and the SOI layer is formed by about 1.5-micrometer thickness.

[0004]

[Problem(s) to be Solved by the Invention] However, when it is going to form a vertical-mold bipolar transistor and C-MISFET in the same SOI layer, there is a problem from which the optimal thickness of the SOI layer demanded with each device composition is different and to say.

[0005] That is, when it is going to form a vertical-mold bipolar transistor in a SOI layer, it is necessary to secure the space which needs to form an emitter, the base, and a collector in lengthwise [of a SOI layer], and forms each semiconductor region. For this reason, from the structure of a vertical-mold bipolar transistor, there is a request of wanting to make thickness of a SOI layer into 1 micrometer to 2 micrometers, for example, 1.5 micrometers.

[0006] It is desirable to constitute MISFET from a partial depletion type or a perfect depletion type on the other hand, if highly efficient-ization of MISFET is taken into consideration when forming MISFET on a SOI layer. It is necessary to set thickness of a SOI layer to 0.1 micrometers or less with 4 micrometers or less and a perfect depletion type with a partial depletion type then.

[0007] In Bi-CMOS device given in the aforementioned reference, SOI layer thickness is arranged with the thickness from which it is requested from bipolar transistor structure, and the channel field of MISFET is not formed into a perfect depletion. for this reason, if the property of MISFET removes an isolation property, the big improvement in comparison with Bulk MISFET will not be found, but the merit made into SOI and MISFET structure is reduced -- things -- **

[0008] For this reason, in order to optimize both the properties of a bipolar transistor and MISFET, it is necessary to optimize the SOI layer membrane in which both devices are formed according to device structure. That is, the SOI thickness of a bipolar portion needs to form SOI thickness of a MISFET portion thinly (for example, 0.4 micrometers or less), while thickening (for example, 0.8 micrometers or more).

[0009] However, if SOI thickness is changed by the substrate field in this way, un-arranging [that a big level difference occurs in the boundary portion, LSI manufacturing processes, such as a photolithography, become difficult, and high integration becomes difficult as a result] will arise.

[0010] The purpose of this invention is to offer flat device structure and the manufacture method without the level difference in the border area, constituting the silicon layer thickness of a bipolar portion or a MISFET portion from thickness suitable for the device structure.

[0011] The other purposes and the new feature will become clear from description and the accompanying drawing of this specification at the aforementioned row of this invention.

[0012]

[Means for Solving the Problem] It will be as follows if the outline of a typical thing is briefly explained among invention indicated in this application.

[0013] That is, the semiconductor device of this invention makes SOI layer thickness thin according to the thickness (for example, 0.4 micrometers or less) of which it is required at partial depletion type or perfect depletion type MISFET. After the bipolar section *****'s the oxide film of the SOI layer lower part, forms opening and forms a collector embedding layer in the silicon substrate of the lower part, it grows the silicon layer used as an active layer epitaxially into the upper layer, and secures thickness required for a bipolar transistor to it.

[0014] Moreover, the sidewall which consists of an insulator layer is formed in the aforementioned opening. By existence of this sidewall, the crystallinity of the silicon layer to grow epitaxially can be made good. Moreover, the silicon layer to grow epitaxially is formed more thickly than the front face of the substrate in which opening was formed, is ground by the CMP method after that, and can carry out flattening.

[0015] In addition, it will be as follows, if this invention is divided into a term and explained.

[0016] 1. the Manufacture Method of Semiconductor Device of this Invention -- (a) Support Substrate Top -- the [1st Insulating Layer and] -- Process Which Deposits 2nd Insulating Layer on SOI Substrate Which Has 1 Silicon Layer -- (b) Etch into the 1st field of a SOI substrate and the 2nd insulating layer, the 1st silicon layer, and the 1st insulating layer are removed alternatively. An epitaxial grown method is given to the process and (c) SOI substrate which form opening which exposes the support substrate of the 1st field. the process which forms the 2nd silicon layer in the silicon front face of an opening pars basilaris ossis occipitalis alternatively, the process which removes the (d) 2nd insulating layer, and (e) -- the the 1st and] -- it has the process which forms an isolation region in 2 silicon layers, forms MISFET in the 1st silicon layer and forms a bipolar transistor in the 2nd silicon layer

[0017] 2. It is the manufacture method of the semiconductor device term 1 publication, and has the process which forms the sidewall which becomes the side attachment wall of opening from an insulator before the (c) process.

[0018] 3. while being the manufacture method of a semiconductor device a term 1 or given in two, making the altitude of the 2nd silicon layer front face higher than the altitude of the 2nd insulating-layer front face in the (c) process and performing removal of the 2nd insulating layer using the CMP method in the (d) process -- a part of 2nd silicon layer -- grinding -- the the 1st and] -- carry out flattening of the front face of 2 silicon layers

[0019] Semiconductor Device of this Invention on the Same Substrate 4. Bipolar Transistor, The 1st silicon layer which is the semiconductor device with which MISFET was formed and by which the substrate was formed through the 1st insulating layer on the support substrate which becomes the front face from single crystal silicon, the 2nd silicon layer which grew epitaxially through the insulating layer on the support substrate -- having -- the [the 1st and] -- flattening of the front face of 2 silicon layers is carried out, MISFET is formed in the 1st silicon layer, and the bipolar transistor is formed in the 2nd silicon film

[0020] 5. the semiconductor device of term 4 publication -- it is -- the [the 1st insulating layer and] -- the spacer which consists of an insulator is formed in the border area of 1 silicon layer and the 2nd silicon layer

[0021] 6. It is a semiconductor device a term 4 or given in five, the 1st silicon layer thickness is 0.4 micrometers or less, and the 2nd silicon layer thickness is 0.8 micrometers or more.

[0022] 7. It is Semiconductor Device of Term 6 Publication, and 1st Silicon Layer Thickness is 0.2 Micrometers or Less. The 1st composition in which the pars basilaris ossis occipitalis of the isolation region formed in the 1st silicon layer has reached the 1st insulating layer of the 1st silicon layer lower part, The 1st silicon layer thickness is 0.1 micrometers or more 0.4 micrometers or less, and the pars basilaris ossis occipitalis of the isolation region formed in the 1st silicon layer has which composition of 2nd composition ** which has not reached the 1st insulating layer of the 1st silicon layer lower part.

[0023] 8. Are Semiconductor Device Given in Any 1 Term of Terms 4-7, and through Insulating Layer on Support Substrate It has further the 3rd silicon layer which grows epitaxially simultaneously with the 2nd silicon layer. The 1st composition with which the impurity of the same conductivity type as a support substrate is introduced into the 3rd silicon layer, and the 4th silicon layer which grows epitaxially simultaneously with the 2nd silicon layer through an insulating layer on a support substrate, It connects with the 4th silicon layer electrically, has further a semiconductor region for the backgates of MISFET formed in the support substrate of the 1st insulating-layer lower part, and has which composition of 2nd composition ** into which the impurity of the same conductivity type as a semiconductor region is introduced in the 4th silicon layer.

[0024]

[Embodiments of the Invention] Hereafter, the gestalt of operation of this invention is explained in detail based on a drawing. In addition, in the complete diagram for explaining the gestalt of operation, the same sign is given to the member which has the same function, and explanation of the repeat is omitted.

[0025] (Gestalt 1 of operation) Drawing 1 - drawing 8 are the cross sections having shown an example of the manufacture method of the semiconductor device of the gestalt 1 of operation in order of the process.

[0026] First, the SOI substrate which embeds on the support substrate 1 and has the silicon layer 3 (SOI layer) of an oxide film 2 and a thin film is prepared. A SOI substrate can be formed by SIMOX (separation by implanted oxygen) etc. The support substrate 1 can be used as the single crystal silicon with which for example, p type impurity was introduced, and the thickness of the embedding oxide film 2 can set it to 0.1 micrometers - 0.5 micrometers. The thickness of the silicon layer 3 carries out to 0.03-0.2 micrometers, for example, 0.06 micrometers. Thus, perfect depletion type MISFET can be formed by making thickness of the silicon layer 3 thin.

[0027] Next, as shown in drawing 1, an insulator layer 4 is formed on the silicon layer 3. Although an insulator layer 4 considers as a silicon oxide, other insulator layers, such as a silicon nitride, are sufficient as it. An insulator layer 4 functions as a growth inhibition layer in the case of epitaxial growth of the single-crystal-silicon film explained later.

[0028] Next, as shown in drawing 2, the insulator layer 4, the silicon layer 3, and the embedding oxide film 2 of the bipolar section (field in which a bipolar transistor is formed) are ***ed alternatively, and opening 5 is formed. Thus, by forming opening 5, support substrate 1 front face is exposed to the pars basilaris ossis occipitalis of opening 5, and epitaxial growth of a single-crystal-silicon film is enabled so that it may explain later. Moreover, since the depth of opening 5 is deeper than the pars basilaris ossis occipitalis of the embedding oxide film 2, let thickness of the single-crystal-silicon film growing epitaxially be sufficient thickness for it to be fully thicker than the silicon layer 3, and form a vertical-mold bipolar transistor. In addition, the aforementioned selective etching can be performed using the technology of a photolithography and anisotropic etching.

[0029] Next, an insulator layer (not shown) is deposited all over a SOI substrate. This insulator layer is deposited so that the wall of opening 5 may be covered. Although an insulator layer considers as a silicon oxide, other insulator layers, such as a silicon nitride, are sufficient as it. However, as for the viewpoint which makes polish speed uniform to an insulator layer, in the polish using the CMP method explained later, it is desirable to make it the same material as the aforementioned insulator layer 4.

[0030] Next, as shown in drawing 3, anisotropic etching is given to this insulator layer and a sidewall 6 is formed in the side attachment wall of opening 5. Thus, since the sidewall 6 which consists of an insulator layer is formed, the karyogenesis of the silicon crystal from the side-attachment-wall portion of opening 5 can be suppressed in the case of epitaxial growth of the single-crystal-silicon film 8 explained later. That is, when a sidewall 6 does not exist temporarily, possibility that the crystallinity of an epitaxial film will deteriorate by the karyogenesis from silicon layer 3 side attachment wall in the stage to which the single-crystal-silicon film (epitaxial film) which has grown epitaxially reached the side attachment wall of the silicon layer 3 is large. However, with the gestalt of this operation in which a sidewall 6 exists, the side attachment wall of opening 5 does not serve as a silicon crystal-growth nucleus, but only an epitaxial growth side serves as a crystalline nucleus, and the single-crystal-silicon film 8 will be tidily formed reflecting the crystallinity of a growth side. Thereby, the crystallinity of the single-crystal-silicon film 8 is kept good.

[0031] Next, as shown in drawing 4, an n type impurity is introduced with ion-implantation, the postheat treatment is performed, and the n type semiconductor region 7 is formed in the support substrate 1 of opening 5 pars basilaris ossis occipitalis. A semiconductor region 7 functions as a collector embedding layer of a bipolar transistor.

[0032] Next, after removing the oxide film of semiconductor-region 7 front face and exposing a single-crystal-silicon front face, the single-crystal-silicon film 8 is formed using an epitaxial grown method. Since fields other than semiconductor-region 7 (support substrate 1) of opening 5 pars basilaris ossis occipitalis are covered by the insulator layer 4 and the sidewall 6, an epitaxial film does not grow up to be this field, but an epitaxial film (single-crystal-silicon film 8) grows up to be it alternatively only inside opening 5. Such a selective growth is realizable by adding chlorine-based gas in the silane system gas which is source gas.

[0033] This single-crystal-silicon film 8 is formed so that it may become high a little rather than the front face of an insulator layer 4. Thus, since facet 8a which is illustrated is formed in the boundary section of that it is desirable to carry out flattening by the CMP method since it does not become even completely, the single-crystal-silicon film 8, and a sidewall 6, if the front face of an epitaxial film forms the single-crystal-silicon film 8 highly and this is ground by the CMP method, it will depend on the reasons [forming highly the front face of the single-crystal-silicon film 8 a little] nil why a facet is removable etc.

[0034] Thus, since an epitaxial film is formed in opening 5, thickness of the single-crystal-silicon film 8 can be made sufficiently thick, and a highly efficient vertical-mold bipolar transistor can be formed in the single-crystal-silicon film 8.

[0035] In addition, since an epitaxial grown method is used also in the general formation process of a bipolar transistor, even if it forms an epitaxial film in opening 5 like the gestalt of this operation, the increase in a process does not necessarily arise as compared with the conventional technology.

[0036] Next, an insulator layer 4, a sidewall 6, and the single-crystal-silicon film 8 are ground using the CMP method and the wet etching method. By this polish, as shown in drawing 5, some of all of insulator layers 4, sidewalls 6, and single-crystal-silicon films 8 are removed, and flattening of the front face of the single-crystal-silicon film 8 and the silicon layer 3 is performed.

[0037] The front face of the single-crystal-silicon film 8 and the silicon layer 3 is mostly formed in the same flat surface so that it may illustrate, and a level difference is not formed in the boundary section. The difficulty on the manufacturing process resulting from a level difference, especially a photolithography process can be removed by this, and a manufacturing process can be made easy. Moreover, as aforementioned, since the single-crystal-silicon film 8 is thickly formed in the interior of opening 5, sufficient thickness to form a vertical-mold bipolar transistor is secured, and, on the other hand, it can form the thickness of the silicon layer 3 in which MISFET is formed by sufficient thin thickness to realize a perfect depletion type.

[0038] In addition, when epitaxial growth can carry out good and the crystallinity of single-crystal-silicon film 8 front face and flat nature can secure sufficiently good, or especially when [even if some level difference exists between the single-crystal-silicon film 8 and the silicon layer 3,] it can approve, it is not necessary to use the CMP method.

[0039] Next, as shown in drawing 6, an isolation region 10 is formed in the field to which an isolation region 9 and a bipolar transistor are formed in the field in which MISFET is formed. Formation of isolation regions 9 and 10 uses the technology of

a photolithography and anisotropic etching for the surface section and the silicon layer 3 of the single-crystal-silicon film 8, forms a slot, and after it deposits the insulator layer which embeds this slot, for example, a silicon oxide, it forms it by removing insulator layers other than Mizouchi using the CMP method or the etchback method.

[0040] The aforementioned slot is simultaneously formed on the both sides of the single-crystal-silicon film 8 and the silicon layer 3. Although etching stops the slot of the silicon layer 3 when it reaches the embedding oxide film 2, since the single-crystal-silicon film 8 is formed more thickly than the silicon layer 3, the slot of the single-crystal-silicon film 8 is formed more deeply than the slot of the silicon layer 3. Therefore, the pars basilaris ossis occipitalis of the isolation region 10 formed in the single-crystal-silicon film 8 is formed lower than the pars basilaris ossis occipitalis of the isolation region 9 formed in the silicon layer 3.

[0041] Next, as shown in drawing 7, the diffusion layer 12 for collector connection is formed in the single-crystal-silicon film 8, and MISFET is formed in the silicon layer 3. The diffusion layer 12 for collector connection is formed by carrying out the ion implantation of the p type impurity by using a photoresist film as a mask, after forming a silicon oxide 11 in the front face of the single-crystal-silicon film 8. MISFET is formed as follows.

[0042] That is, the channel field 21 of p type MISFET and the channel field 22 of n type MISFET are first formed by carrying out the ion implantation of n type impurity and the p type impurity to a predetermined field respectively, using a photoresist film as a mask. Next, the gate insulator layer 13 which removes the silicon oxide 11 on the silicon layer 3, for example, consists of a silicon oxide is formed for example, by the oxidizing [thermally] method. Next, the gate electrode 14 of p type MISFET and the gate electrode 15 of n type MISFET are formed by forming the polycrystal silicon film with which the impurity was introduced, for example, and carrying out patterning of this using a photolithography and etching technology. Under the present circumstances, the so-called dual gate structure of making the conductivity type of the impurity introduced into the gate electrode 14 of p type MISFET and the gate electrode 15 of n type MISFET corresponding to the conductivity type of each MISFET is employable. Next, insulator layers, such as a silicon oxide, are deposited, for example, and a sidewall 16 is formed in the side attachment wall of the gate electrodes 14 and 15 by carrying out anisotropic etching of this. Next, an ion implantation is performed to a predetermined field by using a photoresist film as a mask, and the source diffusion layer 17 of p type MISFET and the drain diffusion layer 18, the source diffusion layer 19 of n type MISFET, and the drain diffusion layer 20 are formed. Thus, n type and p type MISFET are formed in the silicon layer 3.

[0043] Next, as shown in drawing 8, a vertical-mold bipolar transistor is formed in the single-crystal-silicon film 8. Formation of a vertical-mold bipolar transistor is performed as follows.

[0044] First, after removing the silicon oxide 11 on the base and an emitter formation field, an amorphous silicon film is deposited using CVD, for example, boron is poured in with ion-implantation. Next, for example with heat treatment etc., an amorphous silicon film is crystallized and a polycrystal silicon film is formed. Furthermore, a silicon oxide is deposited by CVD on a polycrystal silicon film.

[0045] Next, by using a photoresist film as a mask, etching processing is carried out one by one, and patterning of the aforementioned silicon oxide and the polycrystal silicon film is carried out. This forms the polycrystal silicon film 23 and silicon oxide 37 for base drawers. Then, the ion implantation of the boron of p form impurity is carried out by using the polycrystal silicon film 23 and photoresist film for base drawers as an ion implantation mask. In addition, this boron by which the ion implantation was carried out is diffused with next heat treatment, it serves as an intrinsic base region, and boron (impurity) diffuses it with heat treatment also from the polycrystal silicon film 23 for base drawers, and it serves as a base drawer field of the intrinsic base region circumference. The base-diffusion layer 24 consists of an intrinsic base region and a surrounding base drawer field.

[0046] Next, a silicon oxide is deposited, for example, anisotropic etching of this silicon oxide is carried out, and the sidewall spacer 25 is formed in the side of the polycrystal silicon film 13 for base drawers. Then, after depositing the low resistance polycrystal silicon film containing n form impurity, for example, Lynn, by CVD etc., the polycrystal silicon film 26 for emitter electrodes is formed by carrying out patterning of the low resistance polycrystal silicon film by using a photoresist as an etching mask. Under the present circumstances, a silicon oxide 37 also *****'s simultaneously and exposes polycrystal silicon film 13 front face for base drawers.

[0047] Next, deposit metal membranes, such as titanium, on the whole surface, a silicide reaction is made to cause in the field in which this is heat-treated and titanium and silicon touch, etching removal of the unreacted titanium film is carried out, and the titanium silicide film 28 is formed.

[0048] Then, the insulator layer 29 for passivation which consists of a silicon oxide is deposited, and flattening of this is carried out for example, by the CMP method. Furthermore, a contact hole is formed in an insulator layer 29 by using a photoresist film as a mask, patterning of this after depositing the metal membrane which embeds this contact hole is carried out, and an electrode is formed. An electrode 30 is a base electrode, an electrode 31 is an emitter electrode and an electrode 32 is a collector electrode. Moreover, an electrode 34 is a drain electrode of p type MISFET, an electrode 33 is a source electrode of p type MISFET, and an electrode 36 is [an electrode 35 is a source electrode of n type MISFET, and] a drain electrode of n type MISFET.

[0049] Thus, the semiconductor device of the gestalt of this operation is completed mostly.

[0050] According to the semiconductor device of the gestalt of this operation, thickness of the silicon layer of the bipolar transistor section is thickened, and thickness of the silicon layer of the MISFET section is made thin, and flattening of the substrate is carried out, and high integration of a semiconductor device can be made easy.

[0051] Moreover, since a sidewall 6 is formed, the crystallinity of the single-crystal-silicon film 8 is improved, and the improvement in maintenance of the performance of a bipolar transistor can be carried out good.

[0052] Moreover, since it does not have a SOI layer in the lower part of the bipolar section, the thermolysis property of the bipolar section can be made good. This can avoid the problem of the thermolysis to be increasingly generated with high integration of a bipolar transistor from now on, and shows an effect remarkable in the semiconductor device integrated highly.

[0053] (Gestalt 2 of operation) Drawing 9 - drawing 11 are the cross sections having shown an example of the manufacture method of the semiconductor device of the gestalt 2 of operation in order of the process.

[0054] The semiconductor device of the gestalt of this operation is different from the semiconductor device of the gestalt 1 of operation in the isolation structure of the portion of the bipolar transistor. Since other portions are the same as that of the gestalt 1 of operation, explanation is omitted, and only a different portion is explained.

[0055] The manufacture method of the semiconductor device of the gestalt this operation is the same as that of the process to drawing 6 in the gestalt 1 of operation.

[0056] As shown in drawing 9 after forming the isolation regions 9 and 10 shown in drawing 6 of the gestalt 1 of operation, the slot 52 for isolation is formed in the field in which a bipolar transistor is formed. A slot 52 can be formed by giving anisotropic etching by using a photoresist film as a mask. A slot 52 is formed more deeply than the collector embedding layer 7.

[0057] Next, after oxidizing a silicon layer front face thinly (for example, 5-10nm), the ion implantation of the boron is carried out and the p type channel stop layer 53 is formed.

[0058] Next, as shown in drawing 10, after forming in the whole surface the insulator layer which embeds a slot 52, for example, a silicon oxide, insulator layers other than slot 52 are removed, and an isolation region 54 is formed in a slot 52.

[0059] Then, MISFET and a vertical-mold bipolar transistor are formed like the gestalt 1 of operation (drawing 11).

[0060] According to the semiconductor device of the gestalt of this operation, the element insulation of the bipolar section is made good and the degree of integration of the bipolar section can be improved.

[0061] In addition, as for the thickness of the silicon layer 3 in the case of the gestalt of this operation, it is desirable to be referred to as 0.4 micrometers or less. If it is 0.4 micrometers or less, it is effective in reducing the absorption efficiency of alpha rays and being able to reduce the probability of a soft error.

[0062] (Gestalt 3 of operation) Drawing 12 is the cross section having shown the semiconductor device of the gestalt 3 of operation. The semiconductor device of the gestalt of this operation is made thicker than the gestalt 1 of operation of the thickness of a SOI layer (silicon layer 3), and uses a partial depletion type SOI transistor for MISFET.

[0063] It also leaves the silicon layer 3 to the isolation-region lower part so that it may illustrate. By considering as such composition, the charge accumulated to the channel field through the silicon layer 3 of the isolation-region lower part can be eliminated. Thereby, the performance of MISFET of a semiconductor device is stably maintainable.

[0064] Moreover, the single-crystal-silicon film 8 of the bipolar section and thickness become thick by the relation which thickened thickness of the silicon layer 3. For this reason, the embedding layer 7 can be formed shallowly and the auxiliary collector layer 46 can be formed with an ion implantation etc. Improvement in maintenance of the performance of a bipolar transistor can be aimed at by the auxiliary collector layer 46.

[0065] (Gestalt 4 of operation) Drawing 13 is the cross section having shown the semiconductor device of the gestalt 4 of operation. The semiconductor device of the gestalt of this operation forms the silicon layer 47 formed simultaneously with the single-crystal-silicon film 8 growing epitaxially. The silicon layer 47 can introduce the same impurity as the conductivity type of a substrate, and can be made to act as conductive member for giving potential to substrate potential. The electrode 48 connected to the silicon layer 47 is formed like other electrodes 30-36, potential is given to an electrode 48, and potential can be given to a substrate. Thereby, improvement in a performance of a semiconductor device can be aimed at.

[0066] (Gestalt 5 of operation) Drawing 14 is the cross section having shown the semiconductor device of the gestalt 5 of operation. The semiconductor device of the gestalt of this operation not only gives potential to substrate potential, but has the diffusion layer 50 which gives the back bias of MISFET like the gestalt 4 of operation. A substrate can introduce the impurity of a reverse conductivity type, and when a substrate is p type, Lynn of for example, n type impurity, an arsenic, etc. are poured in with the ion-implantation of a high energy, and it can form them in a diffusion layer 50. A diffusion layer 50 is formed directly under the embedding oxide film 2. Moreover, the silicon layer 49 which touches a diffusion layer 50 can be formed like the silicon layer 47 of the single-crystal-silicon film 8 of the gestalt 1 of operation, or the gestalt 4 of operation, the impurity of the same conductivity type as a diffusion layer 50 can be introduced, and it can be made to act as connection material for connecting with a diffusion layer 50 electrically. The electrode 51 connected to the silicon layer 49 is formed like other electrodes 30-36, potential is given to an electrode 51, and backgate bias can be given. Thereby, improvement in a performance of a semiconductor device can be aimed at. In the case of the gestalt of this operation, although the difficulty of controlling an element property only by structure of MISFET increases when MISFET is especially constituted from a perfect depletion type, since a back bias can be given according to the diffusion layer 50 which acts as a backgate, property control of MISFET becomes easy and the effect can be acquired notably.

[0067] As mentioned above, although invention made by this invention person was concretely explained based on the gestalt of implementation of invention, it cannot be overemphasized by this invention that it can change variously in the range which is not limited to the gestalt of the aforementioned implementation and does not deviate from the summary.

[0068] For example, a bipolar transistor can be replaced with a npn type and let it be a pnp type. In this case, the suitable thing which can be chosen cannot be overemphasized in the conductivity type of a substrate or a diffusion layer.

[0069] Moreover, with the gestalt of the above-mentioned implementation, although the bipolar transistor was formed after formation of MISFET, after forming a bipolar transistor, you may form MISFET. It can be chosen by whether which element property is thought as important whether which transistor element is formed behind. Generally, the element property of the direction formed behind can form good.

[0070]

[Effect of the Invention] It will be as follows if the effect acquired by the typical thing among invention indicated in this application is explained briefly.

[0071] That is, flat device structure and the manufacture method without the level difference in the border area can be offered, constituting the silicon layer thickness of a bipolar portion or a MISFET portion from thickness suitable for the device structure, if this invention is caused.

[Translation done.]

Wakayama

* NOTICES *

Japan Patent Office is not responsible for any damages caused by the use of this translation.

1. This document has been translated by computer. So the translation may not reflect the original precisely.
2. **** shows the word which can not be translated.
3. In the drawings, any words are not translated.

DESCRIPTION OF DRAWINGS

[Brief Description of the Drawings]

[Drawing 1] It is the plan having shown an example of the semiconductor integrated circuit equipment which is the gestalt of 1 operation of this invention.

[Drawing 2] It is an II-II line cross section in drawing 1.

[Drawing 3] It is the cross section having shown an example of the manufacture method of the semiconductor integrated circuit equipment of the gestalt 1 of operation in order of the process.

[Drawing 4] It is the cross section having shown an example of the manufacture method of the semiconductor integrated circuit equipment of the gestalt 1 of operation in order of the process.

[Drawing 5] It is the plan having shown an example of the manufacture method of the semiconductor integrated circuit equipment of the gestalt 1 of operation in order of the process.

[Drawing 6] It is the cross section having shown an example of the manufacture method of the semiconductor integrated circuit equipment of the gestalt 1 of operation in order of the process, and the 01-01 line cross section in drawing 5 is shown.

[Drawing 7] It is the cross section having shown an example of the manufacture method of the semiconductor integrated circuit equipment of the gestalt 1 of operation in order of the process, and the 01-01 line cross section in drawing 5 is shown.

[Drawing 8] It is the plan having shown an example of the manufacture method of the semiconductor integrated circuit equipment of the gestalt 1 of operation in order of the process.

[Drawing 9] It is the cross section having shown an example of the manufacture method of the semiconductor integrated circuit equipment of the gestalt 1 of operation in order of the process, and the 14-14 line cross section in drawing 5 is shown.

[Drawing 10] It is the cross section having shown an example of the manufacture method of the semiconductor integrated circuit equipment of the gestalt 1 of operation in order of the process, and the 14-14 line cross section in drawing 5 is shown.

[Drawing 11] It is the plan having shown an example of the manufacture method of the semiconductor integrated circuit equipment of the gestalt 1 of operation in order of the process.

[Drawing 12] 411-411 [in / drawing 11 / it is the cross section having shown an example of the manufacture method of the semiconductor integrated circuit equipment of the gestalt 1 of operation in order of the process, and] A line cross section is shown.

[Drawing 13] It is the plan having shown an example of the manufacture method of the semiconductor integrated circuit equipment of the gestalt 1 of operation in order of the process.

[Drawing 14] It is the cross section having shown an example of the manufacture method of the semiconductor integrated circuit equipment of the gestalt 1 of operation in order of the process, can set to drawing 13, and is .410-410. A line cross section is shown.

[Drawing 15] It is the cross section having shown an example of the manufacture method of the semiconductor integrated circuit equipment of the gestalt 1 of operation in order of the process, can set to drawing 13, and is .410-410. A line cross section is shown.

[Drawing 16] It is the plan having shown other examples of the semiconductor integrated circuit equipment which is the gestalt of 1 operation of this invention.

[Drawing 17] It is the cross section having shown an example of the semiconductor integrated circuit equipment which is the gestalt of other operations of this invention.

[Drawing 18] It is the cross section having shown an example of the manufacture method of the semiconductor integrated circuit equipment of the gestalt 2 of operation in order of the process.

[Drawing 19] It is the cross section having shown an example of the manufacture method of the semiconductor integrated circuit equipment of the gestalt 2 of operation in order of the process.

[Drawing 20] It is the cross section having shown an example of the manufacture method of the semiconductor integrated circuit equipment of the gestalt 2 of operation in order of the process.

[Drawing 21] It is the cross section having shown an example of the manufacture method of the semiconductor integrated circuit equipment of the gestalt 2 of operation in order of the process.

[Drawing 22] It is the cross section having shown an example of the manufacture method of the semiconductor integrated circuit equipment of the gestalt 2 of operation in order of the process.

[Drawing 23] It is the cross section having shown an example of the manufacture method of the semiconductor integrated

circuit equipment of the gestalt 2 of operation in order of the process.

[Drawing 24] It is the cross section having shown an example of the manufacture method of the semiconductor integrated circuit equipment of the gestalt 2 of operation in order of the process.

[Description of Notations]

- 1 SOI Base
- 1a Support base
- 1b Embedding oxidizing zone
- 1c Silicon layer
- 2a Field insulator layer
- 2b Field insulator layer
- 3 Stay Carrier Drawer Layer
- 4 P Well
- 5 N Well
- 6 Gate Insulator Layer
- 7 Gate Electrode
- 8a Impurity semiconductor field
- 8b Impurity semiconductor field
- 9 Channel Field
- 10 Layer Insulation Film
- 11a connection -- a hole
- 11b connection -- a hole
- 11c connection -- a hole
- 11d connection -- a hole
- 12a Gate drawer electrode
- 12c Carrier drawer electrode
- 12d Backgate electrode
- 13 Stay Carrier Drawer Field
- 14 Impurity Semiconductor Field
- 15 Silicon Nitride
- 16 Photoresist
- 17 Oxide Film
- 18 Photoresist
- 19 Isolation Region of Mesa Form
- 20 Vadum Isolation Region
- 21 Silicon Nitride
- 22 Photoresist
- 23 Photoresist
- 24 Vadum
- 25 Silicon Oxide
- Qn N channel MISFET
- Qp P-channel MISFET

[Translation done.]